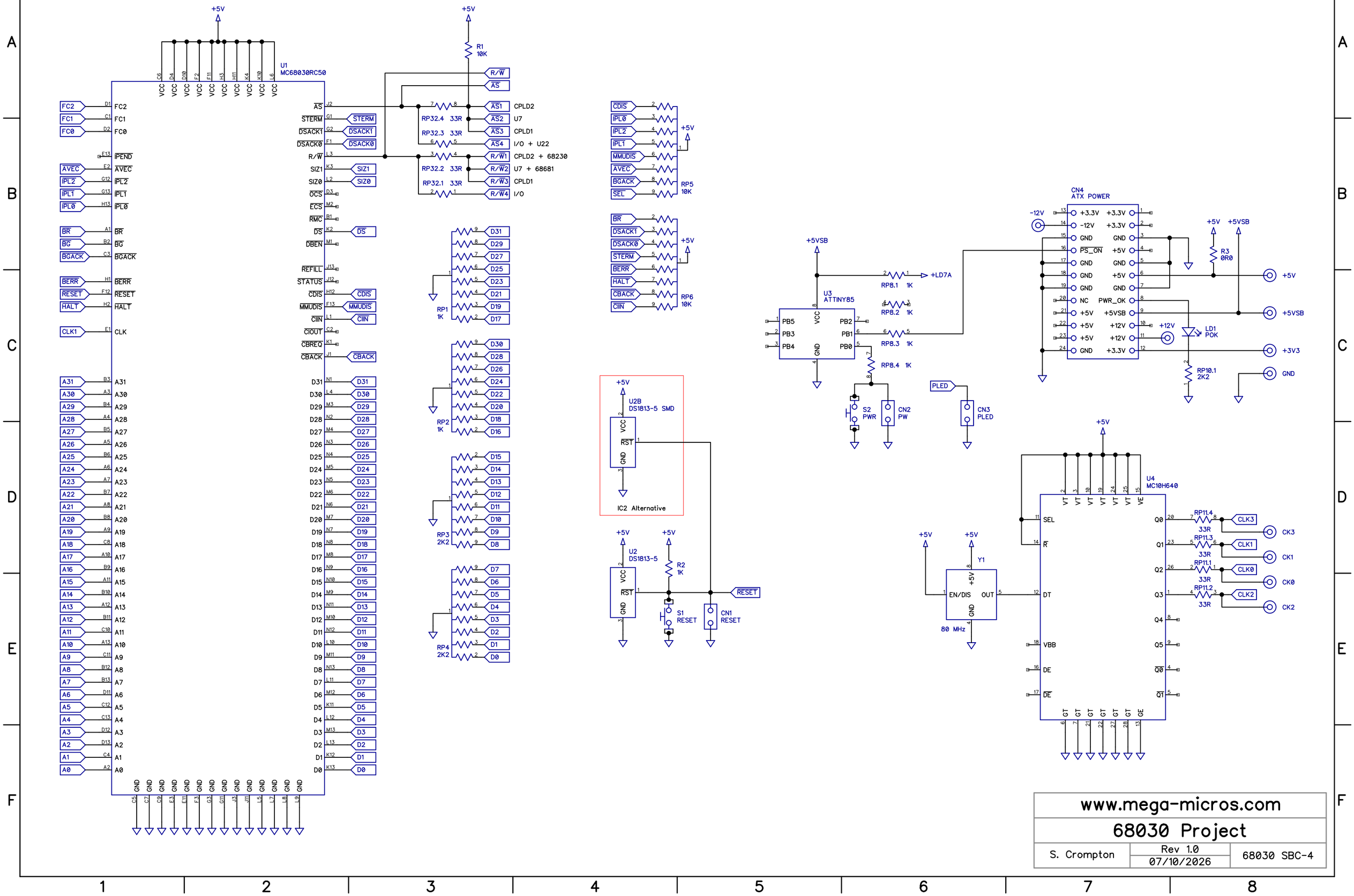
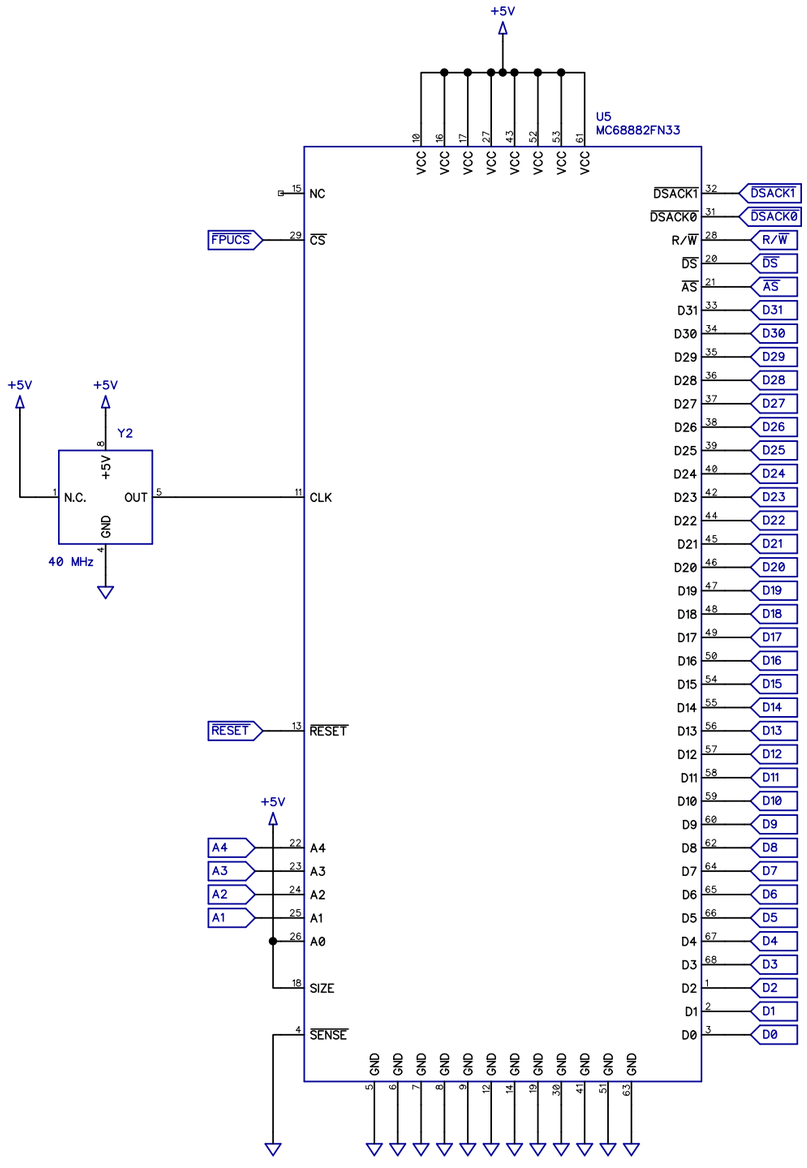
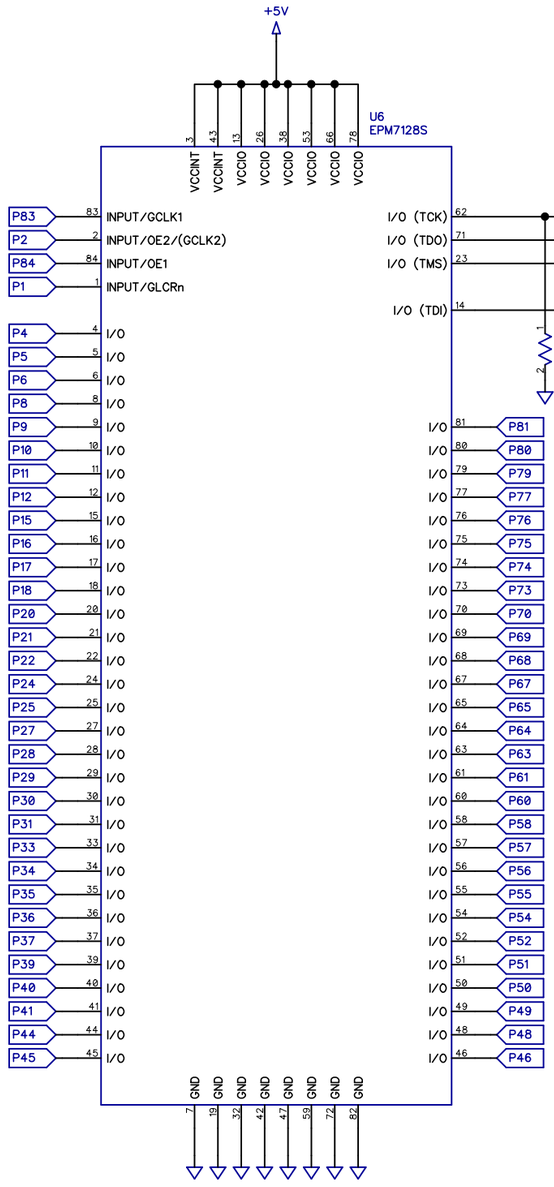
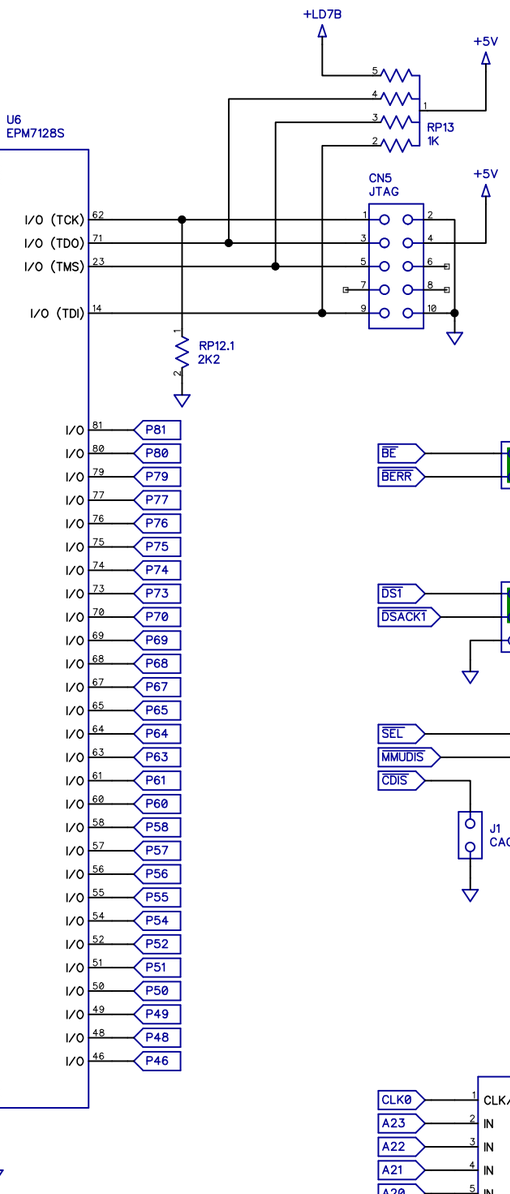
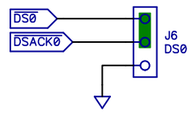

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MC68030RC50
+5V
R1
10K
RP1
1K
RP2
1K
RP3
2K2
RP4
2K2
RP5
10K
RP6
10K
U2B
DS1813-5 SMD
IC2 Alternative
U2
DS1813-5
R2
1K
S1
RESET
CN1
RESET
U3
ATTINY85
RP8.1 1K
RP8.2 1K
RP8.3 1K
RP8.4 1K
+5VSB
+LD7A
S2
PWR
CN2
PW
PLED
CN3
PLED
CN4
ATX POWER
R3
0R0
LD1
POK
RP10.1
2K2
U4
MC10H640
Y1
80 MHz
RP11.4
RP11.3
RP11.1
RP11.2
33R
CK3
CK1
CK0
CK2
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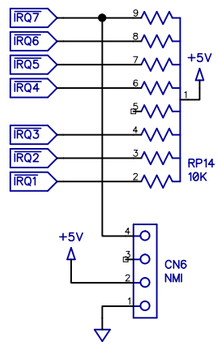


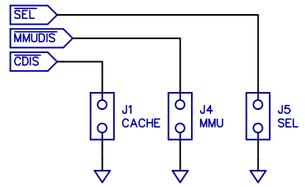
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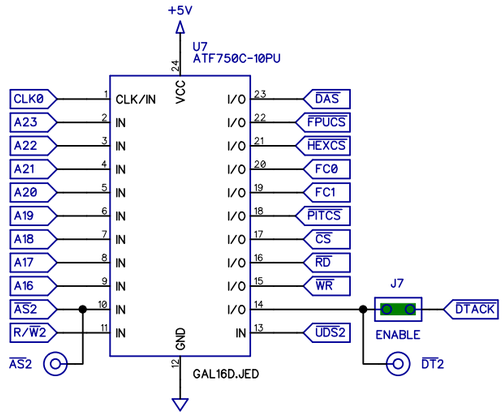


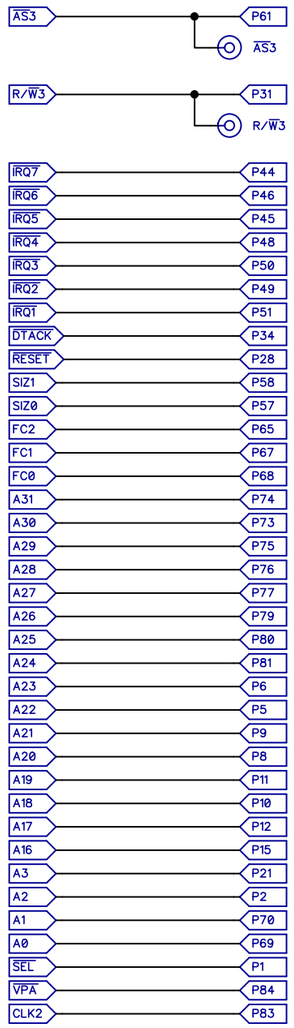


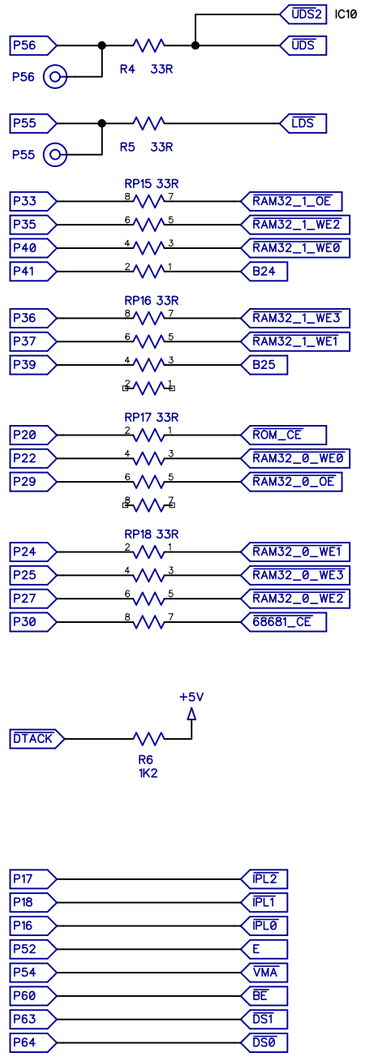








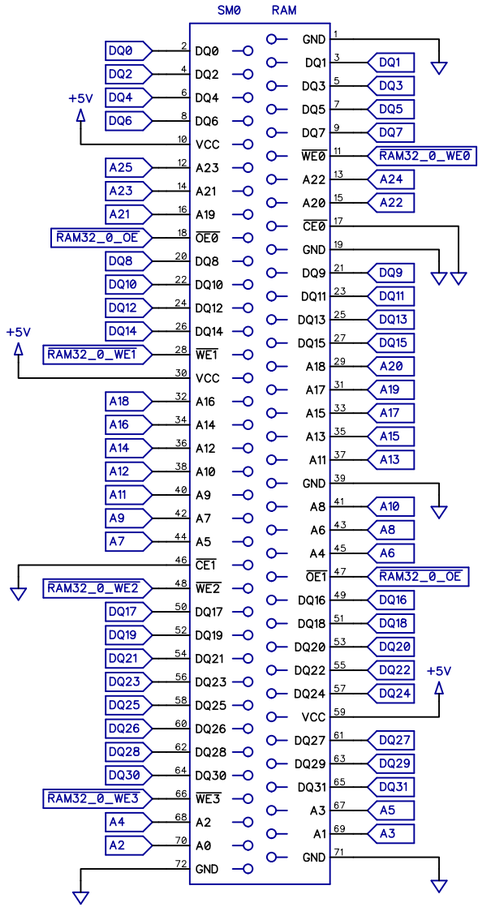




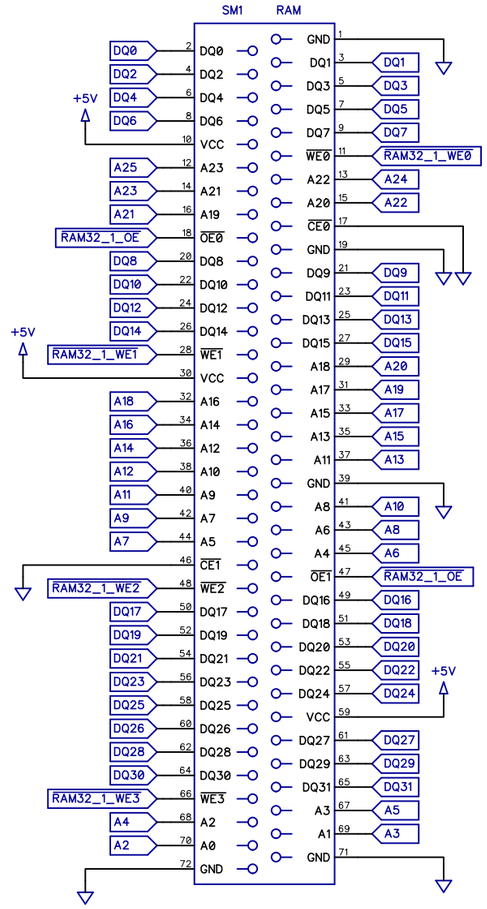


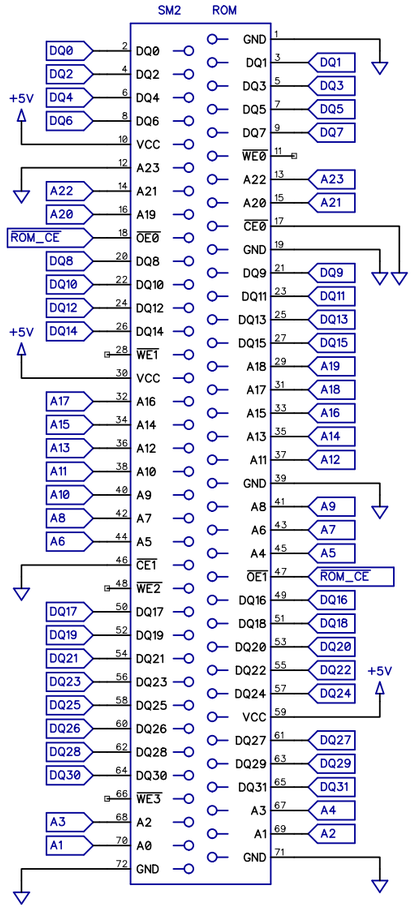
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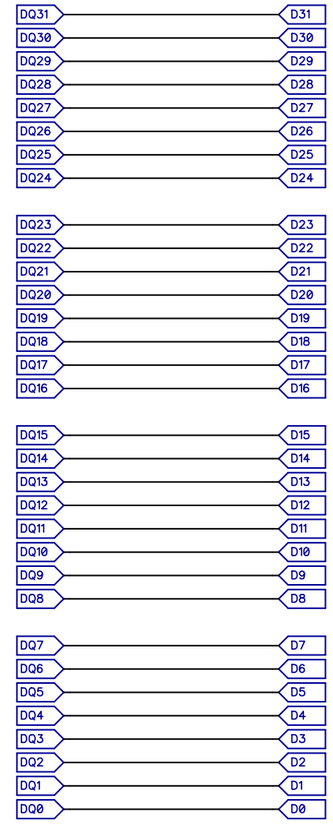
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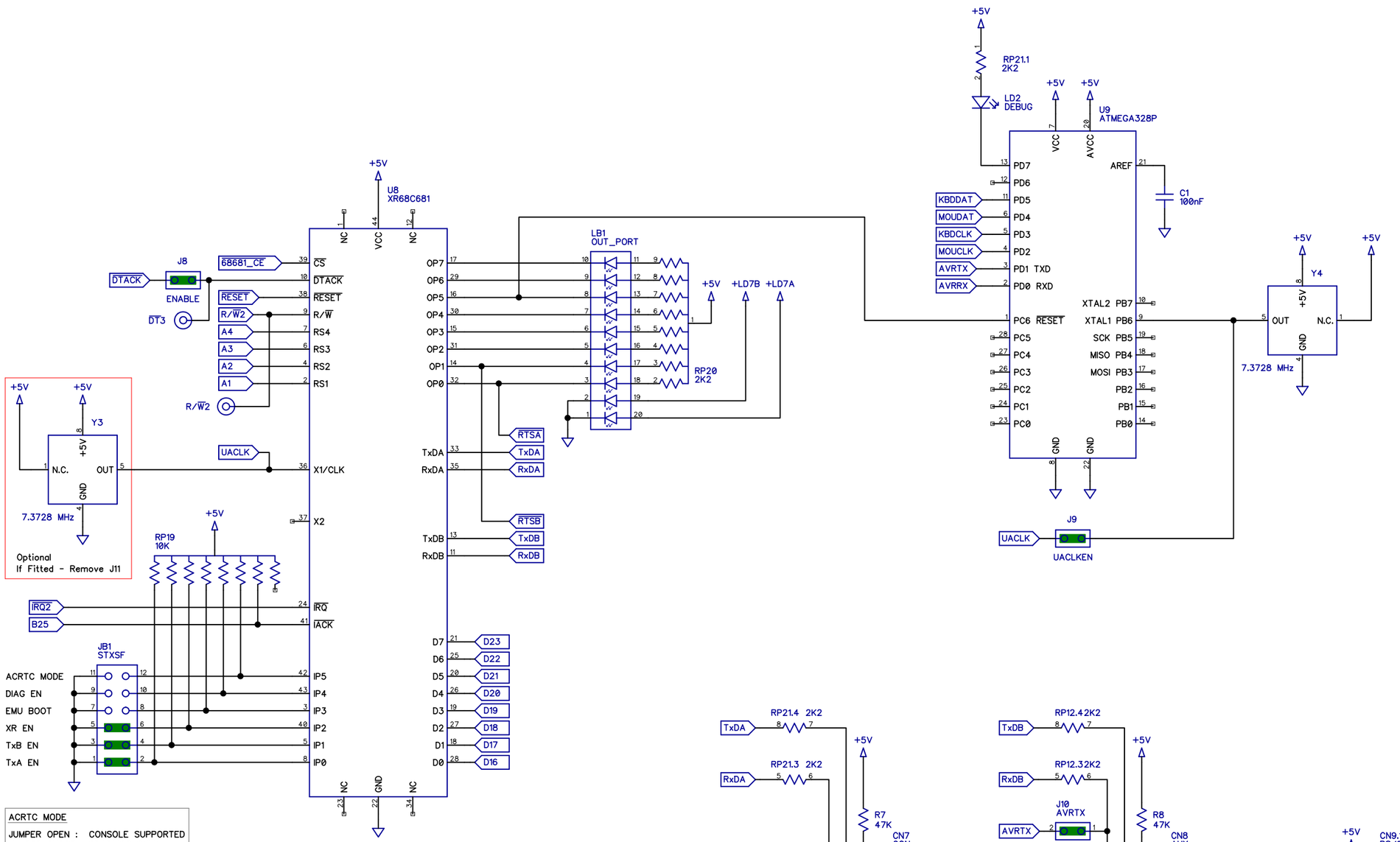
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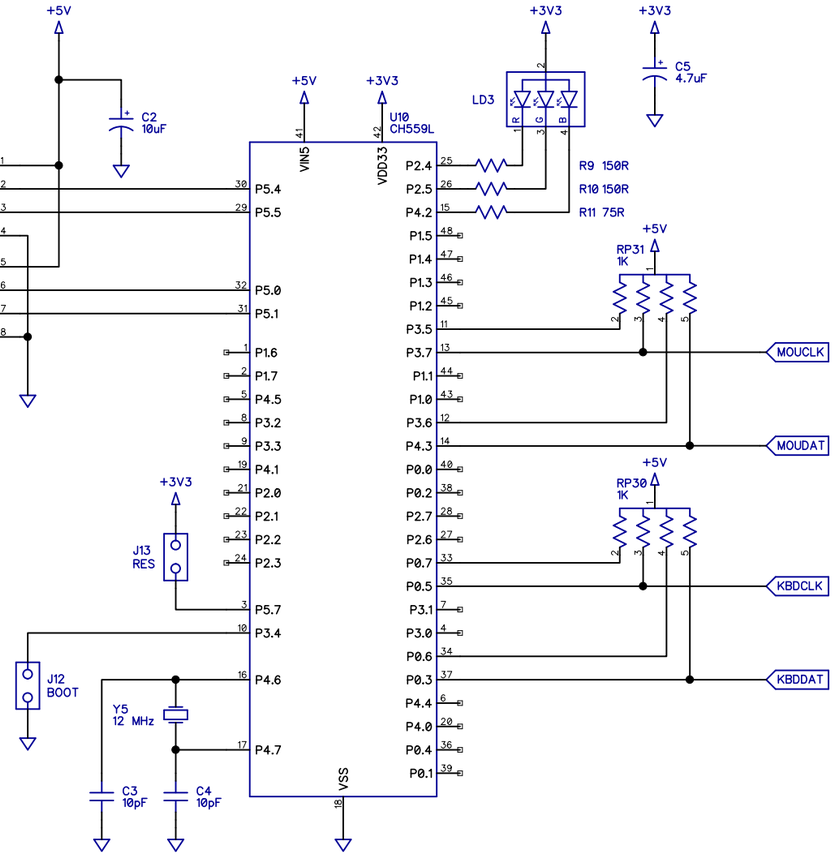




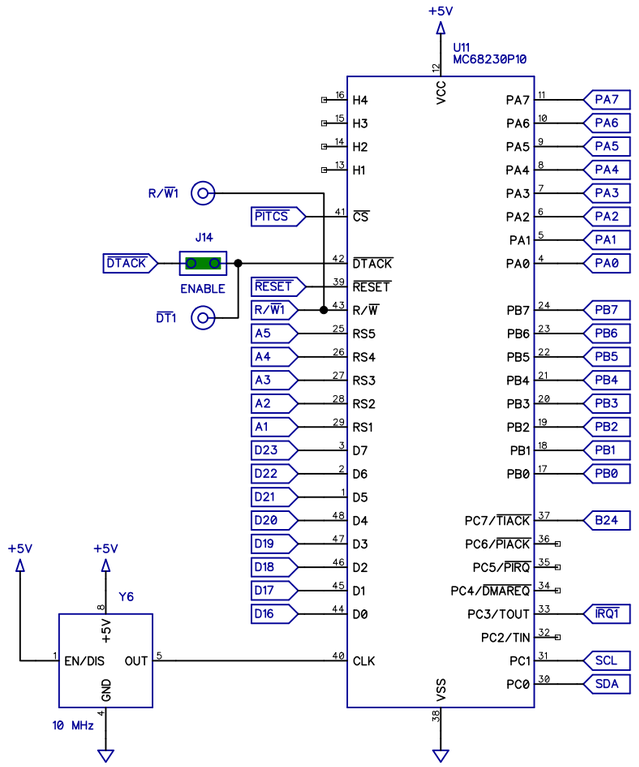
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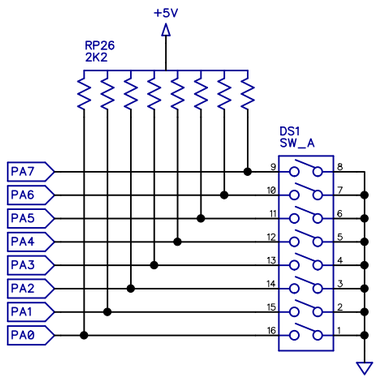


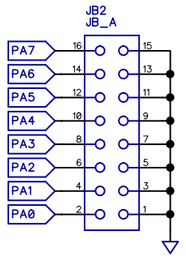
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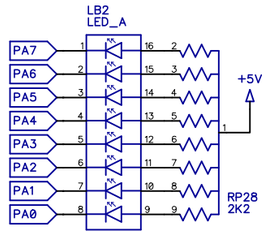


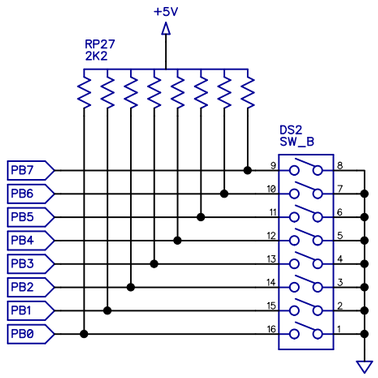
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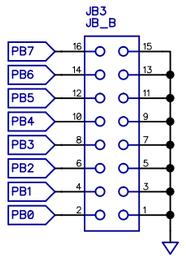


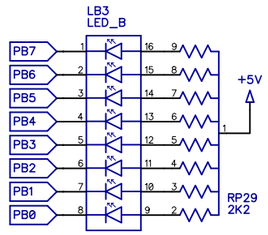


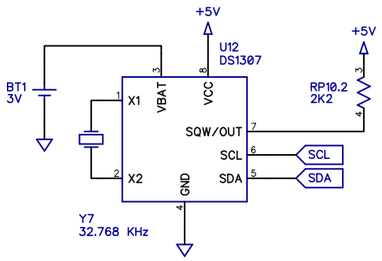


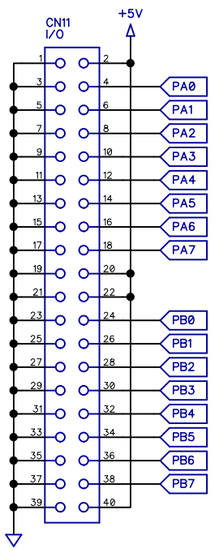


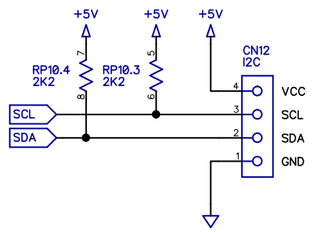




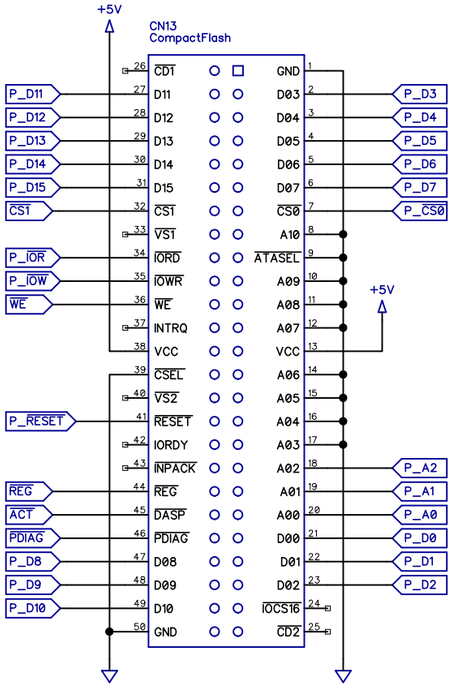


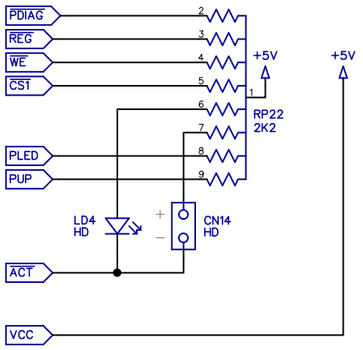


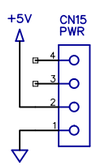


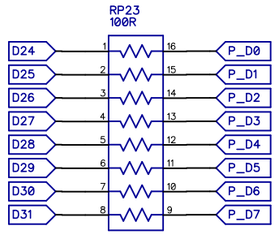


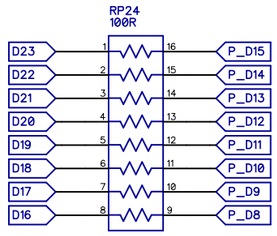
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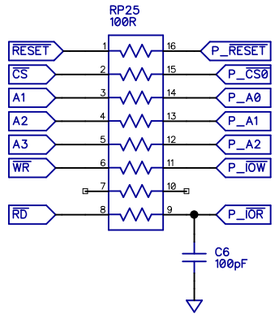


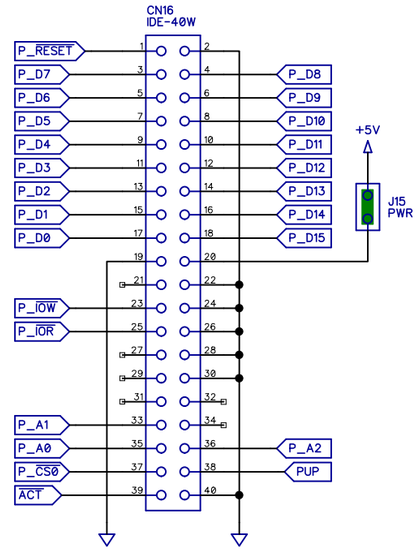


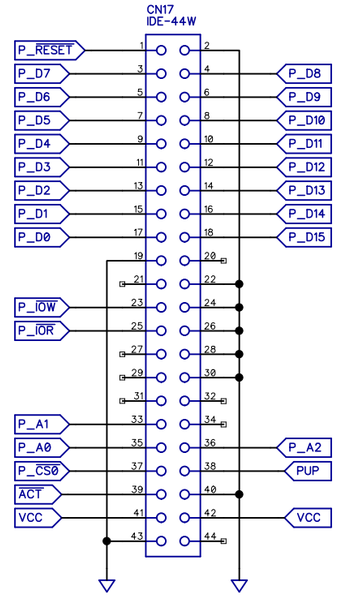




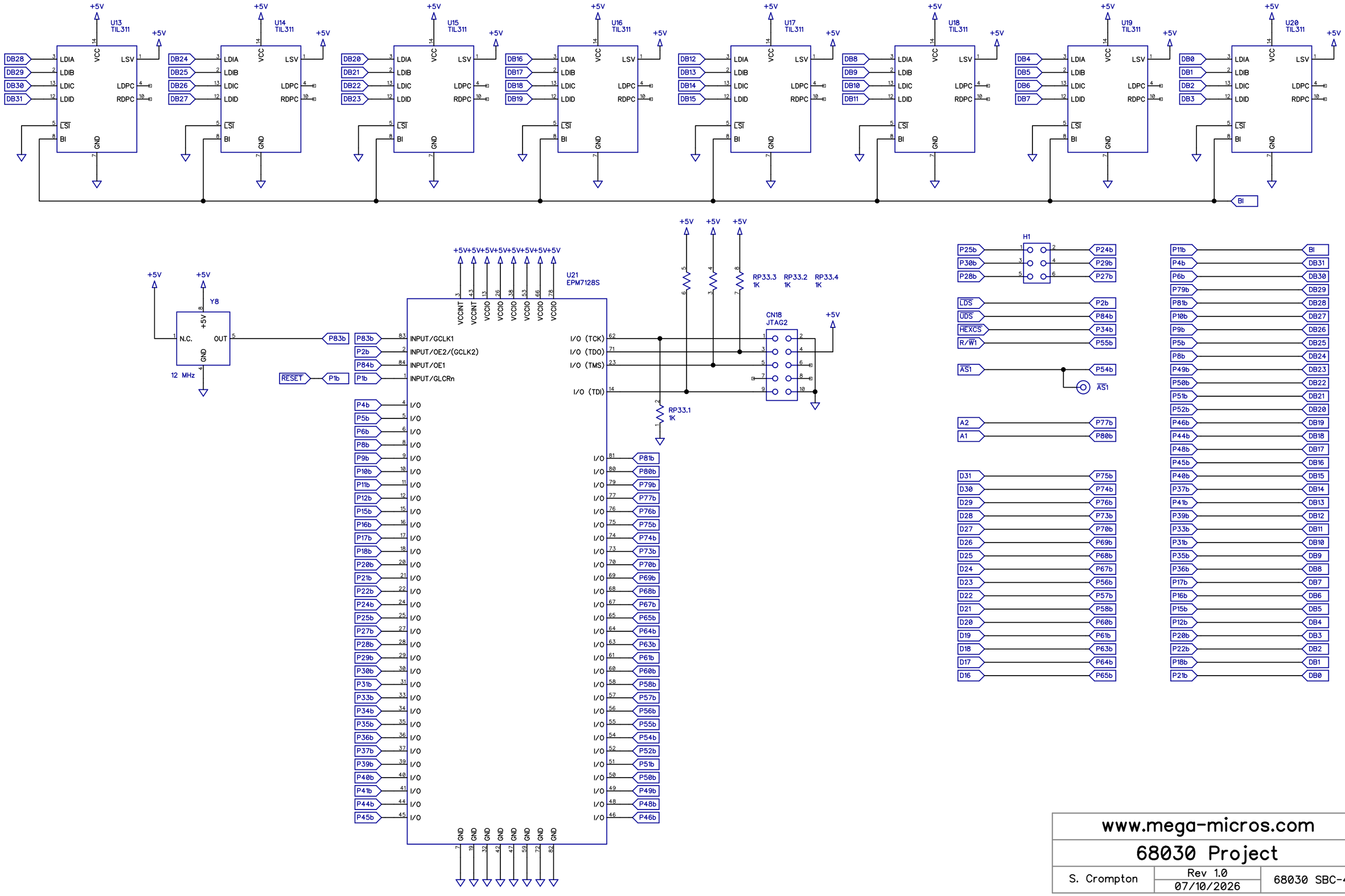




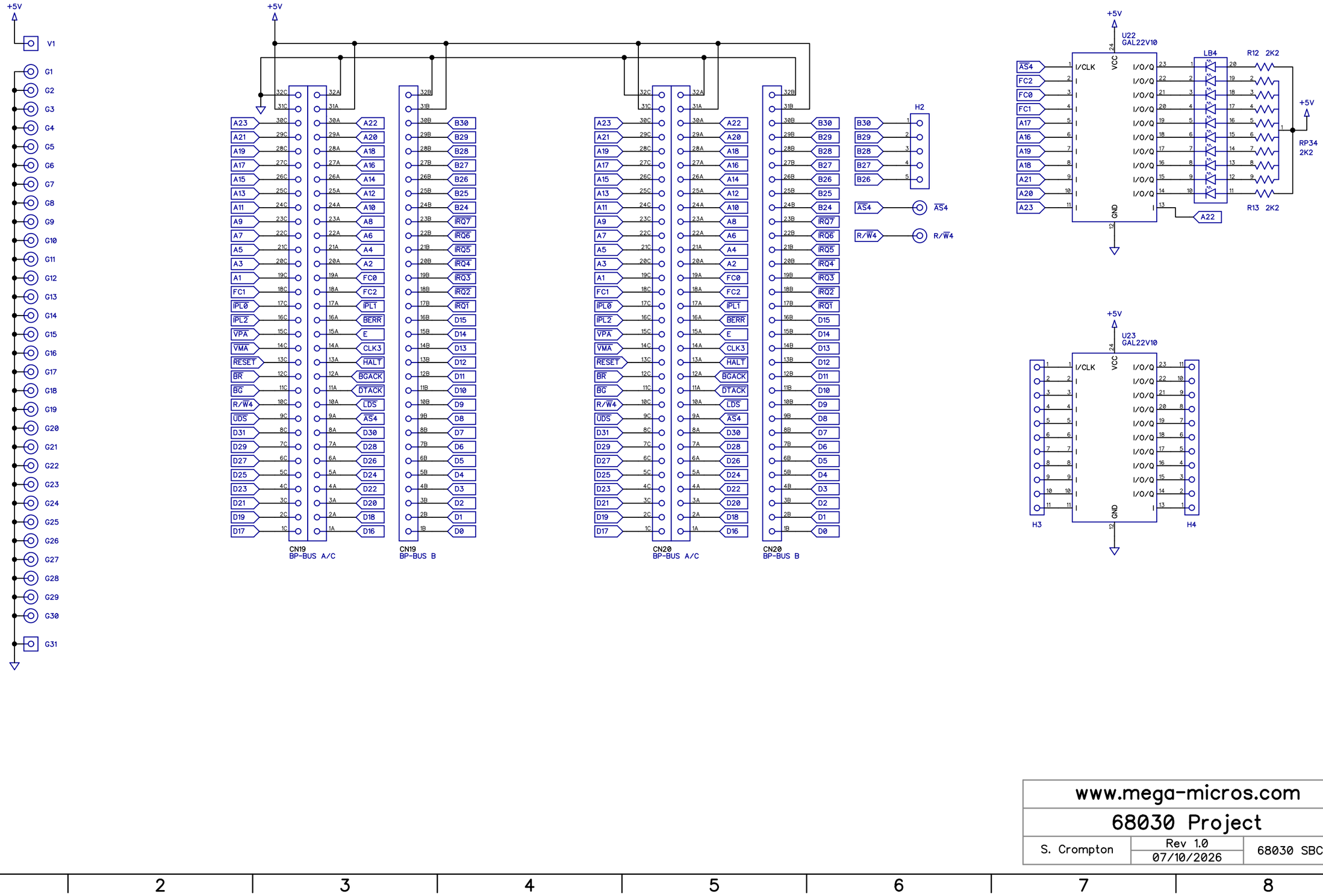




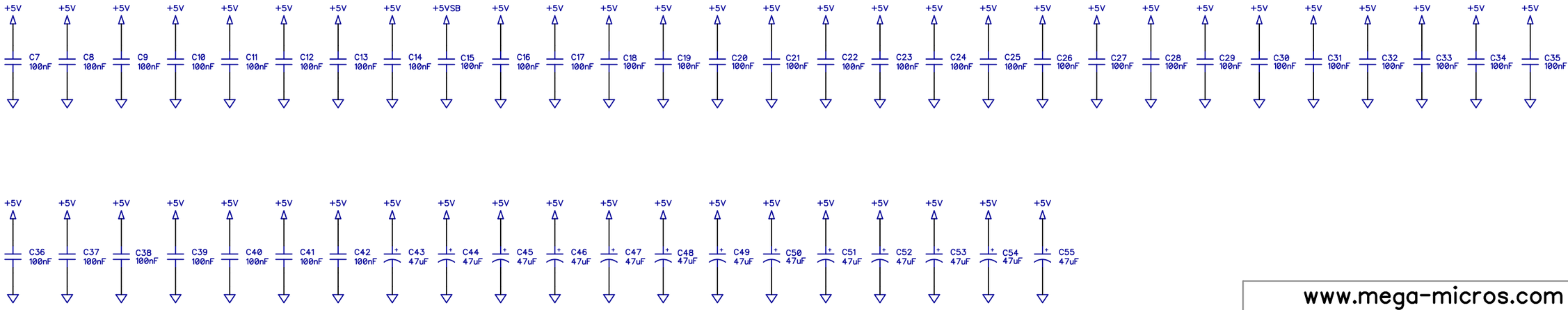
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Change log.

1. Added 47K pull-up resistor to USB1 pin 4
2. Added 47K pull-up resistor to USB2 pin 4
3. AVR reset pin now driven from DUART OP5
4. ATF22V10C GAL replaced with an ATF750C
5. FC0, FC1, $\overline{\text{FPUCS}}$, & $\overline{\text{HEXCS}}$ signals routed to/from pins 20, 19, 22, & 21 of the GAL
6. Requires a delayed $\overline{\text{AS}}$ signal ($\overline{\text{DAS}}$) to be generated by CPLD 1 on P4
7. $\overline{\text{DAS}}$ signal is routed to pin 23 of the GAL
8. Added a second CPLD & 8x TIL311 LED's
9. H1 and P1 removed

Notes:

1. The ATF750C GAL requires GAL16C or GAL16D firmware
2. GAL16C outputs a Coprocessor $\overline{\text{FPUCS}}$ signal on pin 22
3. GAL16D also outputs a Hex Display $\overline{\text{HEXCS}}$ signal on pin 21
4. CPLD 1 requires M80 firmware (or later) - this generates the $\overline{\text{DAS}}$ signal
5. CPLD 2 requires ??? firmware (or later) - this handles the Hex Display

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